

CLAIMS

What is claimed is:

1. A manufacturing process for integrated circuit devices comprising:
storing data and a substantially unique identification code of each integrated circuit device of said integrated circuit devices at one of at probe testing of said integrated circuit devices and after probe testing of said integrated circuit devices, said data indicating a process flow within said manufacturing process for each integrated circuit device of said integrated circuit devices, said storing data comprising:
storing said substantially unique identification code of said each integrated circuit device of said integrated circuit devices and a die location on an electronically stored wafer map for each integrated circuit device;
reading said substantially unique identification code of each integrated circuit device of said integrated circuit devices;
evaluating said data for each integrated circuit device of said integrated circuit devices to said data stored for each integrated circuit device;
identifying integrated circuit devices having a process flow within said manufacturing process different from said process flow of said stored data of said integrated circuit devices; and directing said each integrated circuit device of said integrated circuit devices identified as having a process flow within said manufacturing process different from said process flow of said stored data of said integrated circuit devices to another process.

2. The process of claim 1, wherein said storing data comprises storing data at a probe.

3. The process of claim 1, wherein said storing data comprises storing data and said substantially unique identification code of said each integrated circuit device of said integrated circuit devices to indicate each integrated circuit device of said integrated circuit devices comprises one of a good integrated circuit device and a bad integrated circuit device.

4. The process of claim 1, wherein said reading said identification code of each integrated circuit device of said integrated circuit devices comprises electrically retrieving a unique fuse identification programmed into said each integrated circuit device of said integrated circuit devices.

5. The process of claim 1, wherein said reading said identification code of each integrated circuit device of said integrated circuit devices comprises optically reading a unique identification code on each integrated circuit device of said integrated circuit devices.

6. The process of claim 5, wherein said optically reading said unique identification code provided on each integrated circuit device of said integrated circuit devices comprises optically reading a unique laser fuse identification programmed into each integrated circuit device of said integrated circuit devices.

7. The process of claim 1, wherein said reading said substantially unique identification code of each integrated circuit device of said integrated circuit devices comprises reading said substantially unique identification code of said each integrated circuit device of said integrated circuit devices at an opens/shorts test in said manufacturing process.

8. The process of claim 1, wherein said data stored and said substantially unique identification code of said each integrated circuit device of said integrated circuit devices is accessed by accessing said data stored and said identification code of said each integrated circuit device of said integrated circuit devices at an opens/shorts test in said manufacturing process.

9. The process of claim 8, wherein said evaluating said data comprises evaluating said data accessed for said each integrated circuit device of said integrated circuit devices to identify any bad integrated circuit devices having undergone an assembly procedure within said manufacturing process.

10. The process of claim 8, wherein said evaluating said data comprises evaluating said data at an opens/shorts test in said manufacturing process.

11. The process of claim 1, wherein said directing said each integrated circuit device of said integrated circuit devices identified as having a process flow within said manufacturing process different from said process flow of said stored data of said integrated circuit devices to another process comprises discarding any integrated circuit device identified as having a process flow within said manufacturing process different from said process flow of said stored data.

12. The process of claim 1, wherein said directing occurs before a back-end test procedure within said manufacturing process.

13. The process of claim 1, further comprising assembling said integrated circuit devices into packaged integrated circuit devices after storing data and before reading said substantially unique identification code of said each integrated circuit device of said integrated circuit devices.

14. A method of manufacturing integrated circuit devices comprising:
providing a plurality of semiconductor wafers, each semiconductor wafer having a plurality of integrated circuit devices thereon, said integrated circuit devices comprising:
integrated circuit devices selected from a group comprising Dynamic Random Access Memory (DRAM) devices, Static Random Access Memory (SRAM) devices, synchronous DRAM (SDRAM) devices, and processor devices;
storing a substantially unique identification code in each integrated circuit device of said plurality of integrated circuit devices on said each semiconductor wafer of said plurality of semiconductor wafers;
storing data and said substantially unique identification code of said each integrated circuit device of said plurality of integrated circuit devices indicating manufacturing processes

for said each integrated circuit device of said plurality of integrated circuit devices at one of probe testing and after probe testing of said plurality of integrated circuit devices; separating said each integrated circuit device of said plurality of integrated circuit devices on said each semiconductor wafer of said plurality of semiconductor wafers to form said integrated circuit device of said plurality of integrated circuit devices; assembling said each integrated circuit device of said plurality of integrated circuit devices into an integrated circuit device assembly; reading said substantially unique identification code of said each integrated circuit device of said integrated circuit device assemblies; evaluating data for said each integrated circuit device of said integrated circuit device assemblies identifying any integrated circuit devices having undergone any manufacturing process different from said indicated manufacturing processes of said stored data for said each integrated circuit device; subjecting to further processing said integrated circuit device of said plurality of integrated circuit devices identified as having undergone a manufacturing process different from said indicated manufacturing processes of its stored data; and back-end testing integrated circuit devices not subjected to further processing.

15. The method of claim 14, further comprising programming said each integrated circuit device of said plurality of integrated circuit devices on said each semiconductor wafer of said plurality of semiconductor wafers to permanently store a unique fuse identification.

16. The method of claim 15, wherein said programming said each integrated circuit device of said plurality of integrated circuit devices on said each semiconductor wafer of said plurality of semiconductor wafers to permanently store said unique fuse identification comprises programming at least one of fuses and anti-fuses in said each integrated circuit device of said plurality of integrated circuit devices on said each semiconductor wafer of said plurality of semiconductor wafers to permanently store said unique fuse identification.

17. The method of claim 14, wherein said assembling said each integrated circuit device of said plurality of integrated circuit devices into an integrated circuit device assembly comprises:

 picking each integrated circuit device of said plurality of integrated circuit devices from its semiconductor wafer of said plurality of semiconductor wafers;

 placing said each integrated circuit device of said plurality of integrated circuit devices onto an epoxy-coated bonding site of one of a plurality of lead frames;

 curing said epoxy on said bonding site of each one of said plurality of lead frames;

 wire bonding said each integrated circuit device of said plurality of integrated circuit devices to its associated lead frame;

 injection molding said each integrated circuit device of said plurality of integrated circuit devices and its associated lead frame to form one of a plurality of integrated circuit device packages, each having projecting leads;

 deflashing said projecting leads of each integrated circuit device package of said plurality of integrated circuit device packages;

 curing said each integrated circuit device package of said plurality of integrated circuit device packages;

 electroplating said projecting leads of said each integrated circuit device package of said plurality of integrated circuit device packages;

 singulating said each integrated circuit device package of said plurality of integrated circuit device packages into one of a plurality of discrete integrated circuit devices; and

 testing said each discrete integrated circuit device of said plurality of discrete integrated circuit devices for opens and shorts.

18. The method of claim 14, wherein said assembling said each integrated circuit device of said plurality of integrated circuit devices into an integrated circuit device assembly comprises assembling said each integrated circuit device of said plurality of integrated circuit devices into an integrated circuit device selected from a group comprising a wire bond/lead frame

integrated circuit device, a Chip-On-Board (COB) integrated circuit device, a flip-chip integrated circuit device, and a Tape-Automated Bonding (TAB) integrated circuit device.

19. A method of manufacturing Multi-Chip Modules comprising:

providing a plurality of integrated circuit devices on a semiconductor wafer of a plurality of semiconductor wafers;

storing a substantially unique identification code in each integrated circuit device of said plurality of integrated circuit devices on said each semiconductor wafer at one of probe testing and after probe testing;

storing data and said substantially unique identification code of said each integrated circuit device of said plurality of integrated circuit devices indicating desired manufacturing processes for said each integrated circuit device of said plurality of integrated circuit devices;

separating said each integrated circuit device of said plurality of integrated circuit devices on said each semiconductor wafer of said plurality of semiconductor wafers from said each semiconductor wafer to form one of said plurality of integrated circuit devices;

assembling one or more integrated circuit devices of said plurality of integrated circuit devices into each of a plurality of multi-chip modules, said plurality of multi-chip modules selected from a group comprising Single In-Line Memory Modules (SIMM's) and Dual In-line Memory Modules (DIMM's);

reading said substantially unique identification code of said each integrated circuit device of said plurality of integrated circuit devices in said each of said plurality of multi-chip modules;

evaluating data for said each integrated circuit device of said plurality of integrated circuit devices in said each of said plurality of multi-chip modules identifying any multi-chip modules having integrated circuit devices having undergone a manufacturing process that is different from said desired manufacturing process of said manufacturing processes;

redirecting any multi-chip modules identified as having integrated circuit devices having undergone said manufacturing process that is different from said desired manufacturing process of said manufacturing process; and

back-end testing any nonredirected multi-chip modules.